SUBJECT TEACHING GUIDE

G672 - Computer Architecture and Engineering

Degree in Computer Systems Engineering

Academic year 2016-2017

1. IDENTIFYING DATA			
Degree	Degree in Computer Systems Engineering	Type and Year	Optional. Year 3
Faculty	Faculty of Sciences		
Discipline	Subject Area: Computer Engineering Mention in computer Engingeering		
Course unit title and code	G672 - Computer Architecture and Engineering		
Number of ECTS credits allocated	6	Term	Semester based (2)
Web			
Language of instruction	Spanish	Mode of delivery	Face-to-face

Department	DPTO. INGENIERÍA INFORMÁTICA Y ELECTRÓNICA
Name of lecturer	JOSE ANGEL GREGORIO MONASTERIO
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Other lecturers	PABLO ABAD FIDALGO

3.1 LEARNING OUTCOMES
- To carry out performance evaluation of computers and analyzing the results. Understanding what are the factors affecting the performance and cost. Being able to objectively analyze these factors to justify decision making in the design or purchasing new systems.
- Being able to understand how the technology limitations determine the high complexity of modern memory hierarchies. Being aware of the not negligible influence of the memory hierarchy in software development.
- Understanding how current processors face current technological and cost constraints to maximize computer performance. Being aware of the importance which has the concurrence or instruction level parallelism in order to maximize performance.
- Being able to predict the evolution of computer architecture in the near future.

4. OBJECTIVES

The main objective of the course is to provide students with an accurate picture of how the software interacts with the underlying hardware. The student must acquire an approximate vision of how the processor and memory system of a computer works today.
In particular, it is expected that the student to be able to perform quantitative analysis, using figures of merit, of the performance of a computer running a program and know how to make appropriate comparisons between different design alternatives.
Understanding the concurrent techniques used by today's computers to reduce the execution time. Being aware of the impact on computer performance of taken decisions when programming in a high level language.
Relating the evolution in the integration techniques with the changes undergone by the architecture of computers and how current restrictions will condition the future evolution of computers.

6. COURSE ORGANIZATION

CONTENTS	
1	Computer Design Fundamentals - What is the role of Computer Architecture in the development of computers - Trends and relationships - Metric assessment: parameters and technological bases * Cost * Performance * Energy consumption and Reliability
2	The instruction set The hardware / software boundary Definition and strengths to be pursued by the instruction set: a historical perspective nfluence of compilers and implementation CISC and RISC philosophies
3	Memory hierarchy: caches 3C model in cache misses. Software and hardware prefetch Write policies Evaluation and metrics of the caches Cache Impact on processor performance
4	ILP 1: Segmentation Data dependencies Control dependencies Dynamic branch prediction and speculative execution
5	ILP 2: Superscalar Execution Limits of segmentation Superscalar execution Impact of Multi-Issue Wide-static planning Issue: VLIW Software Planning
6	ILP 3: Dynamic Scheduling Dynamic scheduling algorithms: Precise exceptions and dynamic scheduling and ROB Speculative execution Dependencies between memory access instructions
7	Thread level parallelism. Introduction to the problems of coherence and consistency. Data-level parallelism.
8	Final test

7. ASSESSMENT METHODS AND CRITERIA

Description	Type	Final Eval.	Reassessn	%
Questions and exercises of the whole subject	Written exam	Yes	Yes	45,00
Evaluation of all aspects of development of the labs	Laboratory evaluation	No	Yes	40,00
Midterms	Written exam	No	Yes	15,00
TOTAL				100,00

Observations

Observations for part-time students

Students verifying these conditions and are not examined during the course (or didn't pass lab tests) need to conduct a comprehensive examination. A theoretical part (theory and exercises) written, with a weight of 55% and another part corresponding to the lab with a weight of 45% of the final score.

8. BIBLIOGRAPHY AND TEACHING MATERIALS

BASIC

Título : Microprocessor Architecture: From Simple Pipelines to Chip Multiprocessors
Autor : Jean-Loup Baer,
Editor: Cambridge University Press; 1 edition (December 7, 2009)
ISBN : 0521769922