SUBJECT TEACHING GUIDE

M1709 - Memory Hierarchy

Master's Degree in computing engineering

Academic year 2017-2018

1. IDENTIFYING DATA					
Degree	Master's Degree in computing engineering			Type and Year	Optional. Year 1
Faculty	Faculty of Sciences				
Discipline	Optional Subjects Optional Subjects				
Course unit title and code	M1709 - Memory Hierarchy				
Number of ECTS credits allocated	3	Term		Semester based (2)	
Web					
Language of instruction	Spanish	English Friendly	No	Mode of delivery	Face-to-face

Department	DPTO. INGENIERÍA INFORMÁTICA Y ELECTRÓNICA
Name of lecturer	JOSE ANGEL GREGORIO MONASTERIO
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Other lecturers	

3.1 LEARNING OUTCOMES
- Knowing the relevance of parallel architectures and its use in different application domains.
- Special focus on the memory hierarchy of CMPs (Chip Multiprocessors) .

4. OBJECTIVES
Understand the basic concepts underlying on-chip parallel architectures.
Understanding how communication and synchronization mechanisms of this kind of systems work and how they are related to the programming techniques.
Be knowledgeable of future challenges that these systems must address and the different alternatives that would allow overcome them.

6. COURSE ORGANIZATION

	CONTENTS
1	Introduction to on-chip multiprocessor systems (CMPs)
2	Coherence protocols and consistency models in memory. Motivation. Sequential consistency. TSO consistency. Relaxed consistency. Coherence protocol types. Coding states. Optimizations.
3	On-chip interconnection networks. Characteristics. Interaction network-protocols. Limitations.
4	On-chip and off-chip Scalability of the many-core systems (CMP). General features. Main limitations to scalability.

7. ASSESSMENT METHODS AND CRITERIA

Description	Type	Final Eval.	Reassessn	%
Midterm exam	Oral Exam	No	Yes	50,00
Final test	Written exam	No	Yes	50,00
TOTAL				100,00

Observations
Annual unique test.

Observations for part-time students
Part-time students have the same rules.

8. BIBLIOGRAPHY AND TEACHING MATERIALS

BASIC

Kunle Olukotun, Lance Hammond, James Laudon, "Chip Multiprocessor Architecture: Techniques to Improve Throughput and Latency", Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers, 2007

Natalie Enright Jerger, Li-Shiuan Peh, "On-Chip Networks ", Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers, 2009

Daniel J. Sorin, Mark D. Hill, David A. Wood, "A Primer on Memory Consistency and Cache Coherence". Synthesis Lectures on Computer Architecture. November 2011