

## SUBJECT TEACHING GUIDE

### G1006 - Design of Digital Electronic Systems

#### Degree in Industrial Electronic Engineering and Automatic Control Systems

Academic year 2022-2023

| 1. IDENTIFYING DATA              |   |                  |                    |                  |                    |
|----------------------------------|---|------------------|--------------------|------------------|--------------------|
| Degree                           | Degree in Industrial Electronic Engineering and Automatic Control Systems   |                  |                    | Type and Year    | Compulsory. Year 3 |
| Faculty                          | School of Industrial Engineering and Telecommunications   |                  |                    |                  |                    |
| Discipline                       | Subject Area: Further Digital Electronics<br>Module: Further Specific Technology  |                  |                    |                  |                    |
| Course unit title and code       | G1006 - Design of Digital Electronic Systems  |                  |                    |                  |                    |
| Number of ECTS credits allocated | 6   | Term             | Semester based (1) |                  |                    |
| Web                              | <a href="https://moodle.unican.es/course/view.php?idnumber=G1006_1819">https://moodle.unican.es/course/view.php?idnumber=G1006_1819</a> |                  |                    |                  |                    |
| Language of instruction          | Spanish   | English Friendly | Yes                | Mode of delivery | Face-to-face       |

|                  |   |  |  |  |  |
|------------------|---|--|--|--|--|
| Department       | DPTO. TECNOLOGIA ELECTRONICA E INGENIERIA DE SISTEMAS Y AUTOMATICA                              |  |  |  |  |
| Name of lecturer | EUGENIO VILLAR BONET  |  |  |  |  |
| E-mail           | eugenio.villarb@unican.es   |  |  |  |  |
| Office           | E.T.S. de Ingenieros Industriales y de Telecomunicación. Planta: - 3. DESPACHO PROFESOR (S3098) |  |  |  |  |
| Other lecturers  | IÑIGO UGARTE OLANO  |  |  |  |  |

| 3.1 LEARNING OUTCOMES  |
|--|
| - Ability to describe the desired behavior of digital electronic systems, simulate the description, implement the system and prepare the test. |
| - Capacity to manage existing CAD tools to solve complex problems using FPGAs.   |
| - Ability to operate the necessary instrumentation in an advanced digital electronics laboratory and critically interpret the results.         |
| - Ability to design and apply digital test and analyze and interpret results.  |

#### 4. OBJECTIVES

To provide students with ability to apply the concepts of digital electronics to solve practical problems and work independently.

To provide students the knowledge and skills required to develop industrial applications based on digital electronic systems using FPGA's design environments.

Ability to operate laboratory equipment to verify the performance of the digital system designed and critically interpret the results.

#### 6. COURSE ORGANIZATION

##### CONTENTS

|   |  |
|---|--|
| 1 | Introduction to the design of digital systems<br>Approaches to the design of electronic systems<br>Design process  |
| 2 | Hardware Description Languages at Register-Transfer level<br>Introduction to the VHDL language: CAD tools.<br>Basic elements of the language: structural description, data flow description and behavior description.<br>Design units and VHDL statements.<br>description of Digital Electronic Systems.<br>Management of memories, multipliers and IP blocks. |
| 3 | Verification of Digital Systems<br>Introduction to the Testing of Digital Systems<br>Design for Testability.<br>Reliability of Digital Systems.  |

#### 7. ASSESSMENT METHODS AND CRITERIA

| Description           | Type                  | Final Eval. | Reassessn | %      |
|-----------------------|-----------------------|-------------|-----------|--------|
| Continuous assessment | Others                | No          | Yes       | 20,00  |
| Lab practices         | Laboratory evaluation | No          | Yes       | 50,00  |
| Final exam            | Written exam          | Yes         | Yes       | 30,00  |
| TOTAL                 |                       |             |           | 100,00 |

##### Observations

If the student can not participate in an activity of continuous assessment , the corresponding percentage is added to the percentage of the final exam.

In the case that the health criteria make it necessary, the evaluation tests will be carried out following the mixed teaching format: classroom and non-classroom classes. In the most extreme case that students and teachers cannot go to the classroom, the assessment tests will be carried out using telematic tools. In these cases, the content of the tests, although similar to the face-to-face case, would be totally or partially individualized for each student.

##### Observations for part-time students

The percentage for the continuous assessment activities is added to the percentage of the final exam.

#### 8. BIBLIOGRAPHY AND TEACHING MATERIALS

##### BASIC

Lluís Terés, Yago Torroja, Serafin Olcoz, Eugenio Villar: "VHDL Lenguaje estándar de diseño Electrónico". Mc. Graw Hill

Pong P. Chu: "FPGA Proyotyping by VHDL examples". Wiley Interscience.

