SUBJECT TEACHING GUIDE

G814 - Digital Electronics I

Degree in Telecommunication Technologies Engineering

Academic year 2023-2024

1. IDENTIFYING DATA					
Degree	Degree in Telecommunication Technologies Engineering			Type and Year	Compulsory. Year 2
Faculty	School of Industrial Engineering and Telecommunications				
Discipline	Subject Area: Digital Electronics Module in Common with the Telecommunications Branch				
Course unit title and code	G814 - Digital Electronics I				
Number of ECTS credits allocated	6	Term		Semester based (1)	
Web	https://moodle.unican.es/				
Language of instruction	Spanish	English Friendly	Yes	Mode of delivery	Face-to-face

Department	DPTO. INGENIERÍA INFORMÁTICA Y ELECTRÓNICA
Name of lecturer	MIGUEL ANGEL MANZANO ANSORENA
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Office	Facultad de Ciencias. Planta: + 2. DESPACHO DE PROFESORES (2054)
Other lecturers	

3.1 LEARNING OUTCOMES
- Understanding the Boolean algebra basis and its application to the design of circuits and digital electronic systems.
- Ability to analyze and design combinational circuits.
- Knowledge of the basic memory elements (latches and flip-flops).

4. OBJECTIVES
Mastering the binary representation of data.
Knowing Boolean algebra, logic functions and the building of digital circuits from them.
To know the basic logic elements (logic gates, combinational modules and flip-flops), their representation and their technological features. Use of datasheets.
Design of complex combinational digital circuits from their specifications using basic logic elements.
Use of CAD tools for design and simulation of digital circuits.
Use of electronic equipment for checking the operation of digital circuits.

6. COURSE ORGANIZATION	
CONTENTS	
1	Presentation of the subject. Introduction to digital electronics.
2	Binary Codes. Binary numbers. Binary arithmetic. Binary codes.
3	Logic Functions.
3.1	Switching algebra. Logic operators, logic gates and logic functions. Truth table. Incompletely specified functions. Representation of logic circuits (schematic and introduction to VHDL). Logic analyzer. Logic simulators.
3.2	Logic function minimization. Karnaugh maps. Algorithmic logic synthesis. CAD tools for logic synthesis.
4	Analysis and design of combinational circuits
4.1	Technological parameters. Datasheets. Logic families. Functional and timing analysis of digital circuits. Implementation with logic gates (2-level and multilevel). Implementation with programmable devices.
4.2	Combinational modules. Multiplexers. Decoders. Encoders. Comparators. Adders. Design with combinational logic modules.
5	Sequential Circuits. Introduction to sequential circuits. S-R latch. Flip-flops: clock structures and basic types.

7. ASSESSMENT METHODS AND CRITERIA				
Description	Type	Final Eval.	Reassessn	%
Laboratory work (PRA)	Laboratory evaluation	No	Yes	30,00
Partial exams: problem sessions in lecture room (EXP)	Written exam	No	Yes	20,00
Homework (TRA)	Work	No	Yes	20,00
Written final exam (EXF)	Written exam	Yes	Yes	30,00
TOTAL				100,00

Observations

The mark of the written final exam has to be at least 3 over 10, and the weighted final mark of the assesment methods (0.3 * PRA + 0.2 * EXP + 0.2 * TRA + 0.3 * EXF) has to be at least 5 over 10.

Resit exam: written exam (70%) + laboratory practical exam (30%)

Observations for part-time students

Part-time students can choose between following the usual evaluation of the subject or doing a final exam: written exam (70%) + laboratory practical exam (30%)

8. BIBLIOGRAPHY AND TEACHING MATERIALS

BASIC

Floyd, T.L. (e-book, 2016, 2006, 2000, 1997). "Fundamentos de Sistemas Digitales". Ed. Prentice/Hall

Morris Mano, M. (e-book, 2013, 2007, 2003, 2001, 1987). "Diseño Digital". Ed. Prentice/Hall

Diapositivas de clase, problemas resueltos, y guiones y manuales de las prácticas