SUBJECT TEACHING GUIDE

G825 - Microprocessors

Degree in Telecommunication Technologies Engineering
First Degree in Telecommunication Technologies Engineering

Academic year 2024-2025

1. IDENTIFYING DATA					
Degree	Degree in Telecommunication Technologies Engineering First Degree in Telecommunication Technologies Engineering			Type and Year	Compulsory. Year 3 Compulsory. Year 3
Faculty	School of Industrial Engineering and Telecommunications				
Discipline	Subject Area: Microprocessors Compulsory Module				
Course unit title and code	G825 - Microprocessors				
Number of ECTS credits allocated	6	Term		Semester based (1)	
Web	https://moodle.unican.es/course/view.php?id=11936				
Language of instruction	Spanish	English Friendly	No	Mode of delivery	Face-to-face

Department	DPTO. INGENIERÍA INFORMÁTICA Y ELECTRÓNICA
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3.1 LEARNING OUTCOMES
- Ability to understand the interconnection between the different elements of a computer.
- Ability to understand all input/output processes of a computer, choosing the best technique for each communication process.
- Knowledge regarding the memory hierarchy and its impact on performance.
- Knowledge about the design of single-cycle and pipelined processors, that will allow understanding how different instructions are managed in the processor.

4. OBJECTIVES

The goal is that the students know and understand the fundamentals that drive the operation of the basic elements of a computer, especially those related to Computer Organization. This includes the interconnection between the various elements of the system, including peripherals and input/output, the memory hierarchy and main memory, and the design of the control and data paths of single-cycle and segmented processors.

6. SUBJECT PROGRAM

CONTENTS	
1	Interconnection and I/O: Concept, structure and types of buses; Single bus architecture; Bus hierarchy; Bus protocols; I/O system structure; Scheduled, Interrupt and Direct Memory Access based I/O.
2	Main memory: DRAM memory organization; Memory controller and commands; DRAM timings.
3	Memory Hierarchy: Concept of Memory Hierarchy; Allocation Policies; Replacement Policies; Cache Performance
4	The Single-Cycle Processor: Format of the ISA; Data and Control Path; A simple implementation.
5	The segmented processor: Concept of segmentation; Segmented instruction processing; Control in segmentation; Data hazards and forwarding; Data hazards and deadlocks; Control hazards and branches.

7. ASSESSMENT METHODS AND CRITERIA

Description	Type	Final Eval.	Reassessn	%
Two laboratory exams.	Activity evaluation with Virtual Media	No	Yes	30,00
A partial eliminatory exam.	Written exam	No	Yes	40,00
A final exam covering the complete subject if the partial was not passed.	Written exam	Yes	Yes	30,00
TOTAL				100,00

Observations

The main and recommended evaluation model is continuous assessment. There will also be final exams for students who do not pass the course or decide not to take this model.

The extraordinary call will consist of a theory and practical exam and a laboratory exam, covering all the contents of the course. The grade of the individual partial exams will not be kept in any case for the extraordinary call. The grade of the practical evaluation, if it is equal or higher than 4, may be retained if the student so wishes.

Observations for part-time students

Part-time students can choose between following the usual continuous assessment or doing final lab an theory exams.

8. BIBLIOGRAPHY AND TEACHING MATERIALS

BASIC

Computer Organization and Design RISC-V Edition: The Hardware Software Interface. David A. Patterson, John L. Hennessy. The Morgan Kaufmann Series in Computer Architecture and Design. 2021.

Organización y Arquitectura de Computadores. W. Stallings. 7a Edición. Prentice-Hall, 2006.

Memory Systems: Cache, DRAM, Disk. Bruce Jacob, David Wang, Spencer Ng. Morgan Kaufman. 2007.